PCI8603
User's Manual

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Contents

Chapter 1 Overview

In the fields of Real-time Signal Processing, Digital Image Processing and others, high-speed and high-precision data acquisition modules are demanded. ART PCI8603 data acquisition module, which brings in advantages of similar products that produced in china and other countries, is convenient for use, high cost and stable performance.

ART PCI8603 is a data acquisition module based on PCI bus. It can be directly inserted into IBM-PC/AT or a computer which is compatible with PCI8603 to constitute the laboratory, product quality testing center and systems for different areas of data acquisition, waveform analysis and processing. It may also constitute the monitoring system for industrial production process.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.
Check for the following items in the package. If there are any missing items, contact your local dealer or sales.
➢ PCI8603 Data Acquisition Board
➢ ART Disk
    a) user's manual (pdf)
    b) drive
    c) catalog
➢ Warranty Card

FEATURES

Analog Input

➢ Input Range：±10V,±5V(default), ±2.5, 0~10V
➢ 12-bit resolution
➢ Sampling Rate: 1S/s~500KS/s
➢ Frequency Formula: sampling frequency= main frequency/the number of frequency division, main frequency = 20MHz, 32-bit frequency division, the number of frequency division range: 40~20000000
➢ Analog Input Mode: 16SE/8DI
➢ Data Read Mode: non-empty, half-full inquiry mode and DMA mode
➢ Memory Depth: 8K word FIFO memory
➢ Memory Signs: full, non-empty and half-full
➢ AD Mode: continuum sampling , grouping sampling
➢ Group Interval: software-configurable, minimum value is sampling period, maximum value is 419430uS
➢ Loops of Group: software-configurable, minimum value is one time , maximum value is 255 times
➢ Board Clock Output Frequency: the real sampling frequency of the current AD
➢ Clock Source: external clock, internal clock(software-configurable)
➢ Trigger Mode: software trigger, hardware trigger(external trigger)
➢ Trigger Type: level trigger , edge trigger
➢ Trigger Direction: negative, positive, either positive or negative
➢ Trigger Source: ATR, DTR
➢ Trigger Source DTR Input Range: standard TTL level
➢ AD Conversion Time: 800ns(max)

- Programmable Gain: 1, 2, 4, 8 (AD8251 default)or 1, 2, 5, 10 (AD8250) or 1, 10, 100,   1000 (AD8253)
- Analog Input Impedance: 10MΩ
- Amplifier Set-up Time: 785nS(0.001%)(max)
- Non-linear error: ±2LSB(Maximum)
- System Measurement Accuracy: 0.01%
- Operating Temperature Range: 0℃~50℃
- Storage Temperature Range: −20℃~70℃

Analog Output
- Output Range: ±10V, ±5V, 0~10V, 0~5V
- 12-bit resolution
- Set-up Time: 600ns (0.01%)
- Update Rate: 1MHz (1us/point), software configuration, configuration range: 0.01Hz ~ 1MHz
- Frequency Formula: sampling frequency= main frequency/the number of frequency division, main frequency = 40MHz, 32-bit frequency division, the number of frequency division range: $40~2^{32}$
- Channel No.: 2-channel
- Output Impedance: 50Ωor 75Ω (Jumper Settings)
- Trigger Source: software, hardware (ART, DTR) trigger
- Trigger Mode: single, continuous, single stepped and Burst trigger
- Trigger Direction: negative, positive, either positive or negative
- Memory Depth:256K word RAM/ch
- Non-linear error: ±1LSB(Maximum)
- Output Error (full-scale): ±1LSB
- Operating Temperature Range: 0℃~50℃
- Storage Temperature Range: - 20℃~70℃

Digital Input
- Channel No.: 8-channel
- Electric Standard: TTL compatible
- High Voltage: ≧2V
- Low Voltage: ≦0.8V

Digital Output
- Channel No.: 8-channel
- Electrical Standard: TTL compatible
- High Voltage: ≧3.8V
- Low Voltage: ≦0.44V
- Power-on Reset

Other features
- Board Clock Oscillation: 40MHz
- Board Dimension: 139mm (L) x 111mm (W)

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Component Layout Diagram
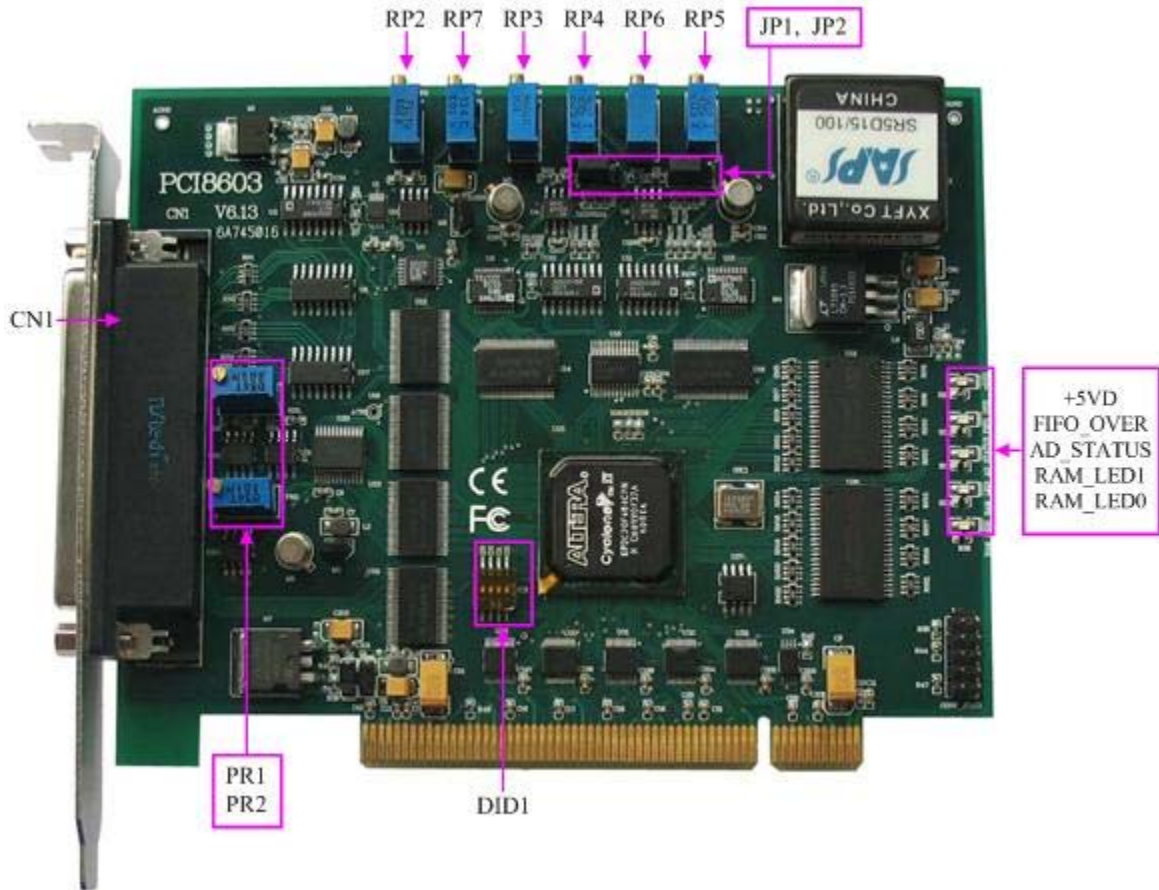
2.2 The Function Description for the Main Component

2.2.1 Signal Input and Output Connectors

CN1:   analog signal input and output connectors

2.2.2 Potentiometer

RP2:   AD analog signal input zero point adjustment potentiometer
RP7:   AD analog signal input full-scale adjustment potentiometer
RP3:   DA0 analog signal output zero point adjustment potentiometer
RP6:   DA1 analog signal output zero point adjustment potentiometer
RP4:   DA0 analog signal output full-scale adjustment potentiometer
RP5:   DA1 analog signal output full-scale adjustment potentiometer
PR1:   trigger level full-scale adjustment potentiometer
PR2:   trigger level zero point adjustment potentiometer

2.2.3 Jumper

JP1~JP2: AO0、AO1 output impedance setting, connect the first and the second pin of the jumper, the output impedance is 75Ω, and connect the second and the third pin, the output impedance is 50Ω.

2.2.4 Status indicator

+5VD: +5V digital power supply indicator, ON for normal condition.
FIFO_OVR: FIFO overflows indicator, ON for FIFO overflow.
AD_STATUS: AD status indicator.
RAM_LED1:   RAM memory indicator.
RAM_LED0:   RAM memory indicator.

## 2.2.5 Physical ID of DIP Switch

DID1: Set physical ID number. When the PC is installed more than one PCI8603 , you can use the DIP switch to set a physical ID number for each board, which makes it very convenient for users to distinguish and visit each board in the progress of the hardware configuration and software programming. The following four-place numbers are expressed by the binary system: When DIP switch points to "ON", that means "1", and when it points to the other side, that means "0." As they are shown in the following diagrams: place "ID3" is the high bit."ID0" is the low bit, and the black part in the diagram represents the location of the switch. (Test software of the company often uses the logic ID management equipments and at this moment the physical ID DIP switch is invalid. If you want to use more than one kind of the equipments in one and the same system at the same time, please use the physical ID as much as possible. As for the differences between logic ID and physical ID, please refer to the function explanations of "CreateDevice" and "CreateDeviceEx" of *The Prototype Explanation of Device Object Management Function* in *PCI8603S* software specification).
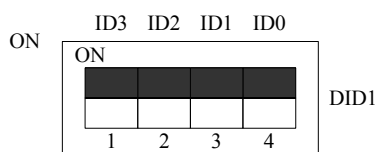
The above chart shows"1111", so it means that the physical ID is 15.
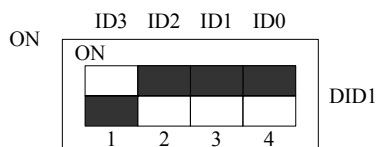
The above chart shows"0111", so it means that the physical ID is 7.
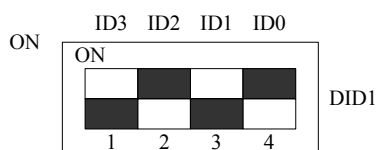
The above chart shows"0101", so it means that the physical ID is 5.

ID3	ID2	ID1	ID0	Physical ID（Hex）	Physical ID（Dec）
OFF（0）	OFF（0）	OFF（0）	OFF（0）	0	0
OFF（0）	OFF（0）	OFF（0）	ON（1）	1	1
OFF（0）	OFF（0）	ON（1）	OFF（0）	2	2
OFF（0）	OFF（0）	ON（1）	ON（1）	3	3
OFF（0）	ON（1）	OFF（0）	OFF（0）	4	4
OFF（0）	ON（1）	OFF（0）	ON（1）	5	5
OFF（0）	ON（1）	ON（1）	OFF（0）	6	6
OFF（0）	ON（1）	ON（1）	ON（1）	7	7
ON（1）	OFF（0）	OFF（0）	OFF（0）	8	8
ON（1）	OFF（0）	OFF（0）	ON（1）	9	9
ON（1）	OFF（0）	ON（1）	OFF（0）	A	10
ON（1）	OFF（0）	ON（1）	ON（1）	B	11
ON（1）	ON（1）	OFF（0）	OFF（0）	C	12
ON（1）	ON（1）	OFF（0）	ON（1）	D	13
ON（1）	ON（1）	ON（1）	OFF（0）	E	14
ON（1）	ON（1）	ON（1）	ON（1）	F	15

Chapter 3 Signal Connectors

3.1 The Definition of Signal Input and Output Connectors

62 core plug on the CN1 pin definition

		21		AI0
		42		AI1
AI2	62	20		AI3
		41		AI4
AI5	61	19		AI6
		40		AI7
AI8	60	18		AI9
		39		AI10
AI11	59	17		AI12
		38		AI13
AI14	58	16		AI15
		37		AGND
AGND	57	15		AGND
		36		AGND
AGND	56	14		DA0
		35		AGND
AGND	55	13		AGND
		34		AGND
ATR	54	12		DA1
		33		AGND
AGND	53	11		AGND
		32		NC
+5VD	52	10		NC
		31		NC
NC	51	9		CLKIN
		30		DGND
CLKOUT	50	8		DTR
		29		DGND
DGND	49	7		DGND
		28		DI0
DI1	48	6		DI2
		27		DI3
DI4	47	5		DI5
		26		DI6
DI7	46	4		DO0
		25		DO1
DO2	45	3		DO3
		24		DO4
DO5	44	2		DO6
		23		DO7
DGND	43	1		DGND
		22		DGND

Pin definition

Signal Name	Type	Definition
AI0~AI15	Input	Analog signal input pins, the reference ground is AGND.
AO0~AO1	Output	Analog signal output pins, the reference ground is AGND.
DI0~DI7	Input	Digital signal input pins, the reference ground is DGND.
DO0~DO7	Output	Digital signal output pins, the reference ground is DGND.
AGND	GND	Analog signal ground.
DGND	GND	Digital signal ground.
CLKIN	Input	External clock input, DGND for reference ground
CLKOUT	Output	Internal clock output, DGND for reference ground
ATR	Input	Analog trigger signal input, AGND for reference ground
DTR	Input	Digital trigger signal input, DGND for reference ground
+5VD	Output	Output 5V power supply
NC		Not connected.

Chapter 4 Connection Ways for Each Signal

4.1 Analog signal single-ended input mode

Single-ended mode can achieve a signal input by one channel, and several signals use the common reference ground. This mode is widely applied in occasions of the small interference and relatively many channels.
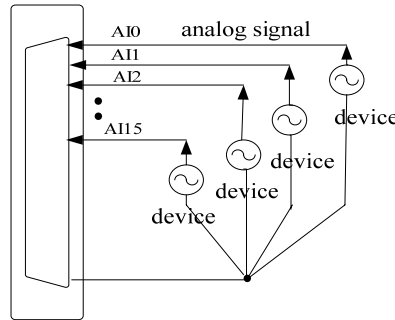

Figure 4.1 single-ended input connection

4.2 Analog signal differential-ended input mode

Double-ended input mode, which was also called differential input mode, uses positive and negative channels to input a signal. This mode is mostly used when biggish interference happens and the channel numbers are few. Single-ended/double-ended mode can be set by the software, please refer to PCI8603 software manual.

According to the diagram below, PCI8603 board can be connected as analog voltage double-ended input mode, which can effectively suppress common-mode interference signal to improve the accuracy of acquisition. Positive side of the 8-channel analog input signal is connected to AI0~AI7, the negative side of the analog input signal is connected to AI8-~AI15, equipments in industrial sites share the AGND with PCI8603 board.
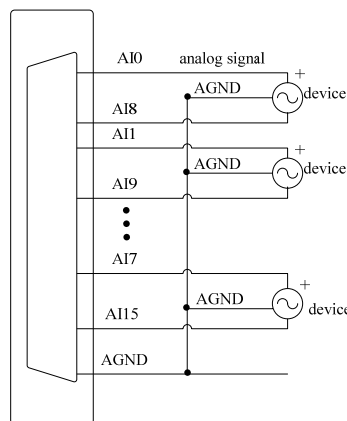

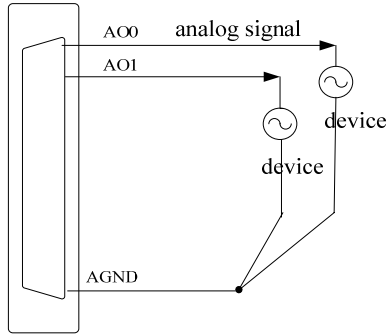*Figure 4.2 Differential-ended input mode*
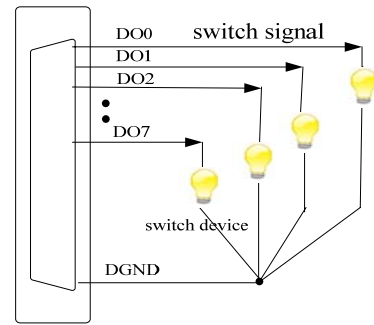
Figure 4.3 analog signal output connection

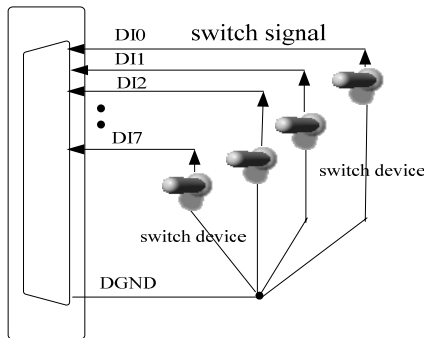*Figure 4.5 digital signal output connection*

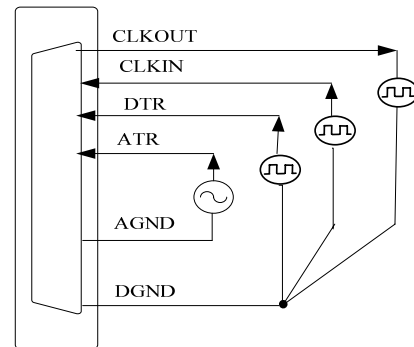*Figure 4.4 digital signal input connection*

*Figure 4.6 Clock Input/Output and Trigger Signal Connection*

4.3 Methods of Realizing the Multi-card Synchronization

Three methods can realize the synchronization for the PCI8603, the first method is using the cascade master-slave card, the second one is using the common external trigger, and the last one is using the common external clock.

When using master-slave cascade card programs, the master card generally uses the internal clock source model, while the slave card uses the external clock source mode. After the master card and the slave card are initialized according to the corresponding clock source mode. At first, start all the slave cards, as the main card has not been activated and there is no output clock signal, so the slave card enters the wait state until the main card was activated. At this moment, the multi-card synchronization has been realized. When you need to sample more than channels of a card, you could consider using the multi-card cascaded model to expand the number of channels.
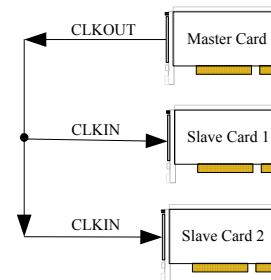
When using the common external trigger, please make sure all parameters of different PCI8603 are the same. At first, configure hardware parameters, and use analog or digital signal triggering (ATR or DTR), then connect the signal that will be sampled by PCI8603, input triggering signal from ART pin or DTR pin, then click "Start Sampling" button, at this time, PCI8603 does not sample any signal but waits for external trigger signal. When each module is waiting for external trigger signal, use the common external trigger signal to startup modules, at last, we can realize synchronization data acquisition in this way. See the following figure:
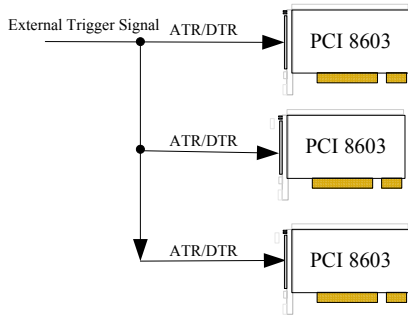
Note: when using the DTR, select the internal clock mode

When using the common external clock trigger, please make sure all parameters of different PCI8603 are the same. At first, configure hardware parameters, and use external clock, then connect the signal that will be sampled by PCI8603, input trigger signal from ART pin or DTR pin, then click "Start Sampling" button, at this time, PCI8603 does not sample any signal, but wait for external clock signal. When each module is waiting for external clock signal, use the common external clock signal to startup modules, at last, we realize synchronization data acquisition in this way. See the following figure:
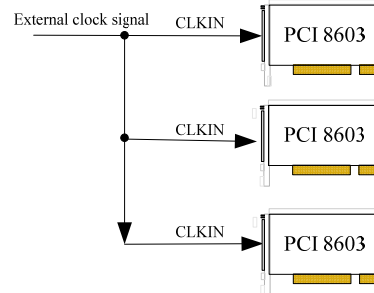
Chapter 5 The Instruction of the AD Trigger Function

5.1 AD Internal Trigger Mode

When AD is in the initialization, if the AD hardware parameter ADPara.TriggerMode = PCI8603_TRIGMODE_SOFT, we can achieve the internal trigger acquisition. In this function, when calling the StartDeviceProAD function, it will generate AD start pulse, AD immediately access to the conversion process and not wait for the conditions of any other external hardware. It also can be interpreted as the software trigger.

As for the specific process, please see the figure below, the cycle of the AD work pulse is decided by the sampling frequency.
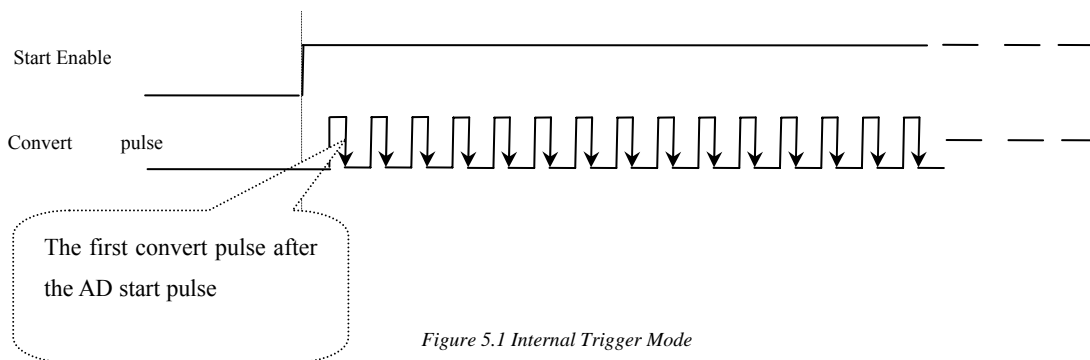

Figure 5.1 Internal Trigger Mode

5.2 AD External Trigger Mode

When AD is in the initialization, if the AD hardware parameter ADPara.TriggerMode = PCI8603_TRIGMODE_POST, we can achieve the external trigger acquisition. In this function, when calling the StartDeviceProAD function, AD will not immediately access to the conversion process but wait for the external trigger source signals accord with the condition, then start converting the data. It also can be interpreted as the hardware trigger. Trigger source includes the DTR (Digital Trigger Source) and ATR (Analog Trigger Source)

When the trigger signal is the digital signal (standard TTL-level), using the DTR trigger source. When the trigger signal is the analog signal, using the ATR trigger source (Trigger level needs to be set when using the ATR trigger source).

The trigger modes include the edge trigger and level trigger. In this manual, we take DTR for example (ATR is the same as DTR).

 (1) Edge trigger function
Edge trigger is to capture the characteristics of the changes between the trigger source signal and the trigger level signal to trigger AD conversion.

When ADPara.TriggerDir = PCI8603_TRIGDIR_NEGATIVE, choose the trigger mode as the falling edge trigger. That is, when the DTR trigger signal is on the falling edge, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition.
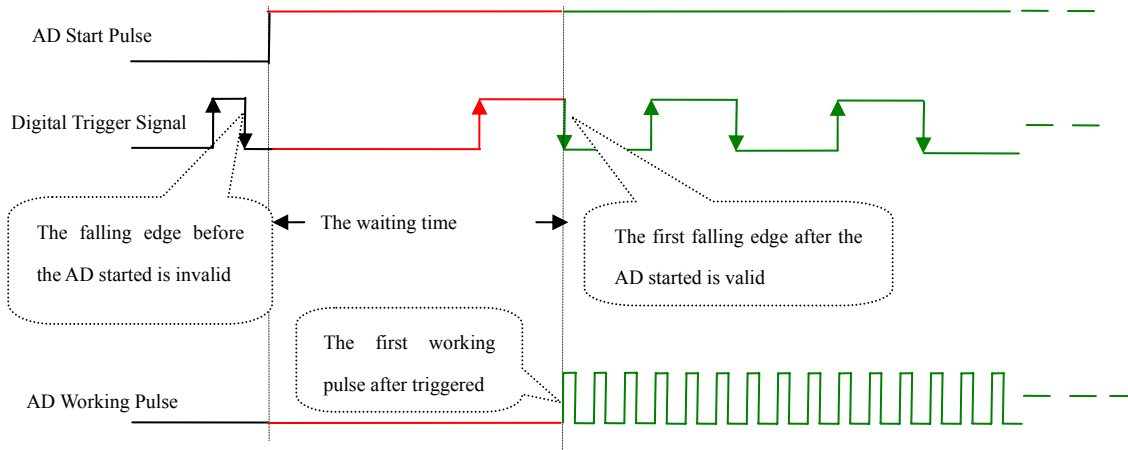

Figure 5.2.1 Falling edge trigger when trigger source is DTR

When ADPara.TriggerDir = PCI8603_TRIGDIR_POSITIVE, choose the trigger mode as rising edge trigger. That is, when the DTR trigger signal is on the rising edge, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition.

When ADPara.TriggerDir = PCI8603_TRIGDIR_POSIT_NEGAT, choose the trigger mode as rising or falling edge trigger. That is, when the DTR trigger signal is on the rising or falling edge, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition. This function can be used in the case that the acquisition will occur if the exoteric signal changes.

（2）**Triggering level function**
Level trigger is to capture the condition that trigger signal is higher or lower than the trigger level to trigger AD conversion.

When ADPara.TriggerDir = PCI8603_TRIGDIR_NEGATIVE, it means the trigger level is low. When DTR trigger signal is in low level, AD is in the conversion process, once the trigger signal is in the high level, AD conversion will automatically stop, when the trigger signal is in the low level again, AD will re-access to the conversion process, that is, only converting the data when the trigger signal is in the low level.

Figure 5.2.2 Low level trigger when trigger source is ATR

When ADPara.TriggerDir = PCI8603_TRIGDIR_POSITIVE, it means the trigger level is high. When DTR trigger signal is in high level, AD is in the conversion process, once the trigger signal is in the low level, AD conversion will automatically stop, when the trigger signal is in the high level again, AD will re-access to the conversion process, that is, only converting the data when the trigger signal is in the high level.
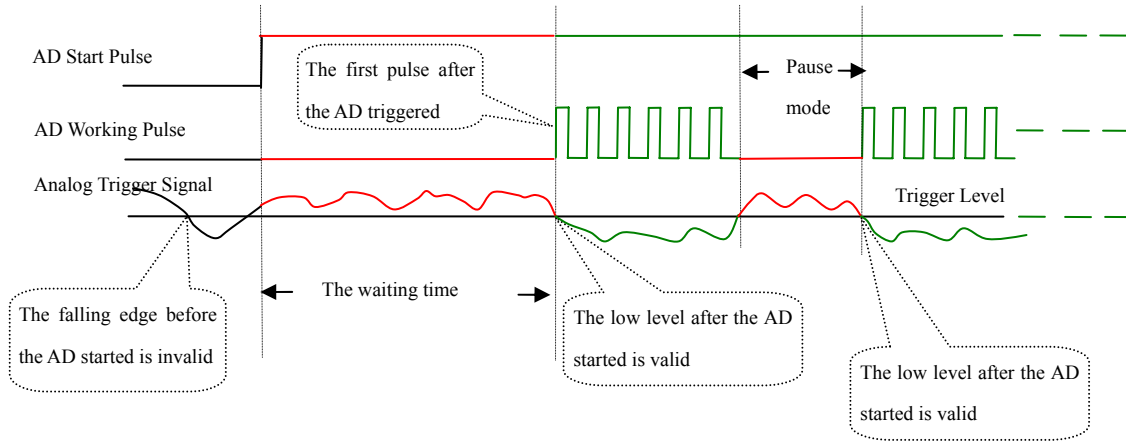
When ADPara.TriggerDir = PCI8603_TRIGDIR_POSIT_NEGAT,the effect is the same as the internal software trigger.

Chapter 6 Methods of using AD Internal and External Clock Function

6.1 Internal Clock Function of AD

Internal Clock Function refers to the use of on-board clock oscillator and the clock signals which are produced by the user-specified frequency to trigger the AD conversion regularly. To use the clock function, the hardware parameters ADPara.ClockSource = PCI8603 _CLOCKSRC_IN should be installed in the software. The frequency of the clock in the software depends on the hardware parameters ADPara.Frequency. For example, if Frequency = 100000, that means AD work frequency is 100000Hz (that is, 100 KHz, 10 μs /point).

6.2 External Clock Function of AD

External Clock Function refers to the use of the outside clock signals to trigger the AD conversion regularly. The clock signals are provide by the CLKIN pin of the CN1 connector.   The outside clock can be provided by PCI8603 clock output (CLKOUT of CN1), as well as other equipments, for example clock frequency generators. To use the external clock function, the hardware parameters ADPara.ClockSource = PCI8603_CLOCKSRC_OUT should be installed in the software. The clock frequency depends on the frequency of the external clock, and the clock frequency on-board (that is, the frequency depends on the hardware parameters ADPara.Frequency) only functions in the packet acquisition mode and its sampling frequency of the AD is fully controlled by the external clock frequency.

6.3 Methods of Using AD Continuum and Grouping Sampling Function

6.3.1 AD Continuum Sampling Function

The continuous acquisition function means the sampling periods for every two data points are completely equal in the sampling process of AD, that is, completely uniform speed acquisition, without any pause, so we call that continuous acquisition.

To use the continuous acquisition function, the hardware parameters ADPara.ADMode = PCI8603 _ADMODE_SEQUENCE should be installed in the software. For example, in the internal clock mode, hardware parameters ADPara.Frequency = 100000 (100KHz) should be installed, and 10 microseconds after the AD converts the first data point, the second data point conversion starts, and then 10 microseconds later the third data point begins to convert, and so on.

6.3.2 AD Grouping Sampling Function

Grouping acquisition (pseudo-synchronous acquisition) function refers to the sampling clock frequency conversion among the channels of the group in the AD sampling process, and also a certain waiting time exists between every two

groups, this period of time is known as the Group Interval. Loops of group refer to numbers of the cycle acquisition for each channel in the same group. In the internal clock mode and the fixed-frequency external clock mode, the time between the groups is known as group cycle. The conversion process of this acquisition mode as follows: a short time stop after the channels conversion in the group (that is, Group Interval), and then converting the next group, followed by repeated operations in order, so we call it grouping acquisition.

The purpose of the application of the grouping acquisition is that: at a relatively slow frequency, to ensure that all of the time difference between channels to become smaller in order to make the phase difference become smaller, thus to ensure the synchronization of the channels, so we also say it is the pseudo-synchronous acquisition function. In a group, the higher the sampling frequency is, the longer Group Interval is, and the better the relative synchronization signal is. The sampling frequency in a group depends on ADPara. Frequency, Loops of group depends on ADPara.LoopsOfGroup, the Group Interval depend on ADPara. Group Interval.

Based on the grouping function, it can be divided into the internal clock mode and the external clock mode. Under the internal clock mode, the group cycle is decided by the internal clock sampling period, the total number of sampling channels, Loops of group and Group Interval together. In each cycle of a group, AD only collects a set of data. Under the external clock mode, external clock cycle ≥ internal clock sampling cycle × the total number of sampling channels × Loops of group + AD chip conversion time, AD data acquisition is controlled and triggered by external clock. The external clock mode is divided into fixed frequency external clock mode and unfixed frequency external clock mode. Under the fixed frequency external clock mode, the group cycle is the sampling period of the external clock.

The formula for calculating the external signal frequency is as follows:

Under the internal clock mode:
Group Cycle = the internal clock sampling period × the total number of sample channels × Loops of group + AD chips conversion time + Group Interval
External signal cycle = (cycle signal points / Loops of group) × Group Cycle
External signal frequency = 1 / external signal cycle

Under the external clock mode: (a fixed-frequency external clock)
Group Cycle = external clock cycle
External signal cycle = (cycle signal points / Loops of group) × Group Cycle
External signal frequency = 1 / external signal cycle

Formula Notes:
The internal sampling clock cycle = 1 / (AD Para. Frequency)
The total number of sampling channels = AD Para. Last Channel – AD Para. First Channel + 1
  Loops of group == ADPara.LoopsOfGroup
  AD Chips conversion time = see "AD Analog Input Function" parameter
  Group Interval = AD Para. Group Interval
Signal Cycle Points = with the display of the waveform signal in test procedures, we can use the mouse to measure the signal cycle points.

Under the internal clock mode, for example, sample two-channel 0, 1, and then 0 and 1 become a group. Sampling frequency (Frequency) = 100000Hz (cycle is 10μs), Loops of group is 1, Group Interval = 50μs, then the acquisition process is to collect a set of data first, including a data of channel 0 and a data of channel 1. We need 10μs to sample the two data, 20μs to convert the data from the two channels. After the conversion time of an AD chip, AD will automatically cut-off to enter into the waiting state until the 50μs group interval ends. We start the next group, begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:

Figure 6.1 Grouping Sampling which grouping cycle No is 1 under the Internal Clock Mode

Note: a— internal clock sample cycle

b— AD chips conversion time

c—Group Interval

d— group cycle

Change the loops of group into 2, then the acquisition process is to collect the first set of data, including two data of channel 0 and two data of channel 1, the conversion order is 0,1,0,1. We need 10μs to sample each of the four data. After the conversion time of an AD chip, AD will automatically stop to enter into the waiting state until the 50μs Group Interval ends. We start the next group, begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:
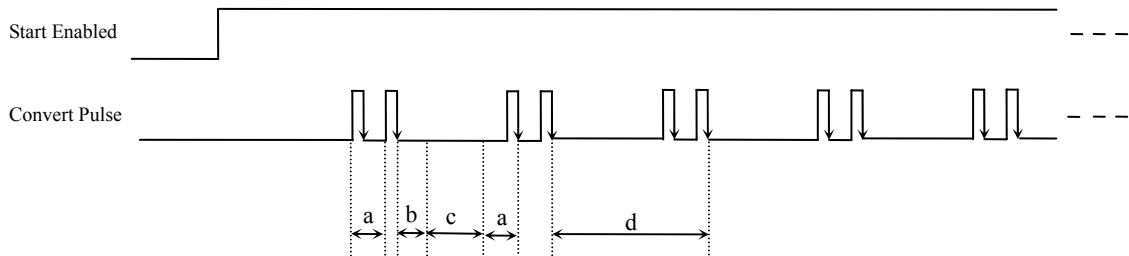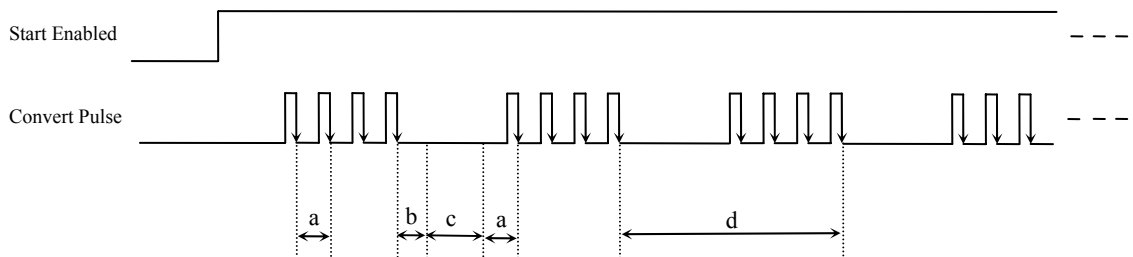

Figure 6.2 Grouping Sampling which grouping cycle No is 2 under the Internal Clock Mode

Notes: a— internal clock sample cycle

b— AD chips conversion time

c—Group Interval

d— group cycle

Under the external clock mode, the requirement is: the external clock cycle ≥ the internal clock sampling period × the total number of sampling channels× Loops of group + AD chip conversion time, otherwise, the external clock appearing in the group conversion time will be ignored.

Under the fixed-frequency external clock mode, for example, when sampling data of two-channel 0, 1, then channel 0 and channel 1 consist of a group. Sampling frequency (Frequency) = 100000Hz (the cycle is 10μs), Loops of group is 2, then the acquisition process is to collect the first set of data, including two data of channel 0 and two data of channel 1, the order of conversion 0,1,0,1, We need 10μs to sample the four data and 40μs to convert of the four data. After the conversion time of an AD chip, AD will automatically stop to enter into the waiting state until the next edge of the external clock triggers AD to do the next acquisition, and the conversion is going on in this way, as the diagram following shows:
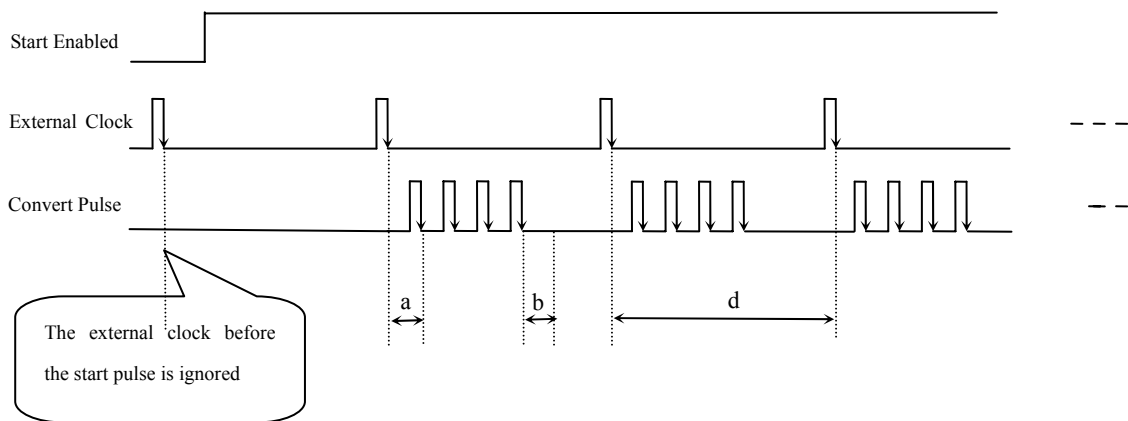

Figure 6.3 Grouping sampling under the fixed frequency external clock mode

Notes: a— internal clock sample cycle
          b—AD chips conversion time
          d—group cycle（external clock cycle）

Under an unfixed-frequency external clock mode, for example, the grouping sampling principle is the same as that of the fixed-frequency external clock mode. Under this mode, users can control any channel and any number of data. Users will connect the control signals with the clock input of the card (CLKIN), set the sampling channels and Loops of group. When there are external clock signals, it will sample the data which is set by users. Because the external clock frequency is not fixed, the size of external clock cycle is inconsistent but to meet: the external clock cycle ≥ the internal clock sampling period × the total number of sampling channels × Loops of group + AD chip conversion time, , otherwise, the external clock edge appearing in the group conversion time will be ignored.
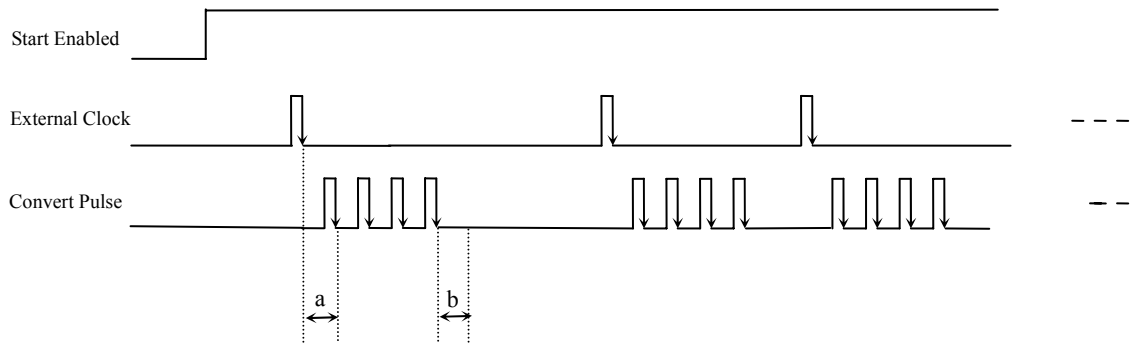
Figure 6.4 Grouping sampling under the not fixed frequency external clock mode

Note: a— internal clock sample cycle

b—AD chips conversion time

6.4 Internal Clock Function of DA

Internal Clock Function refers to the use of on-board clock oscillator and the clock signals which are produced by the user-specified frequency to trigger the AD conversion regularly. To use the clock function, the hardware parameters DAPara.ClockSouce = PCI8603_CLOCKSRC_IN should be installed in the software. The frequency of the clock in the software depends on the hardware parameters DAPara.Frequency. For example, if Frequency = 100000, that means DA output frequency is 100000Hz (that is, 100 KHz, 10 μs /point).

6.5 External Clock Function of DA

External Clock Function refers to the use of the outside clock signals to trigger the AD conversion regularly. The clock signals are provide by the CLKIN pin of the CN1 connector. To use the external clock function, the hardware parameters DAPara.ClockSouce = PCI8603_CLOCKSRC_OUT should be installed in the software. The clock frequency depends on the frequency of the external clock, in external clock mode, the frequency of DA refresh and read wave are the same as external clock.

Chapter 7 Notes, Calibration and Warranty Policy

7.1 Notes

In our products' packing, user can find a user manual, a PCI8603 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using PCI8603, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of PCI8603 module.

7.2 Analog Signal Input Calibration

Every device has to be calibrated before sending from the factory. It is necessary to calibrate the module again if users want to after using for a period of time or changing the input range. PCI8603 default input range: ±5V, in the manual, we introduce how to calibrate PCI8603 in ±5V, calibrations of other input ranges are similar.

Prepare a digital voltage instrument which the resolution is more than 5.5 bit, install the PCI8603 module, and then power on, warm-up for fifteen minutes.

1) Zero adjustment: select one channel of analog inputs, take the channel AI0 for example, connect 0V to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±5V input range and start sampling, adjust potentiometer RP2 in order to make voltage value is 0.000V or about 0.000V. Zero adjustment of other channels is alike.

2) Full-scale adjustment: select one channel of analog inputs, take the channel AI0 for example, connect 4997.55mV to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±5V input range and start sampling, adjust potentiometer RP7 in order to make voltage value is 4997.55mV or about 4997.55mV. Full-scale adjustment of other channels is alike.

3) Repeat steps above until meet the requirement.

7.3 Analog Signal Output Calibration

In the manual, we introduce how to calibrate PCI8603 in ±5V output range; calibrations of other input ranges are similar.

1) Connect the ground of the digital voltage meter to any analog AGND of the CN162 core D-type plug. Connect the input side of the voltage meter to the output channel which needs calibration. Run PCI8603 test procedure under Windows, select the AO output detection.

2) To set AO output is 2048，adjust potentiometer RP3 in order to make DA0 output 0.000V.

3) To set AO output is 4095, adjust potentiometer RP4 in order to make DA0 output 4997.55mV

4) Repeat steps above until meet the requirement.

7.4 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.

2. All ART products come with a limited two-year warranty:

➢ The warranty period starts on the day the product is shipped from ART's factory

➢ For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.

➢ Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:

➢ Damage caused by not following instructions in the User's Manual.

➢ Damage caused by carelessness on the user's part during product transportation.

➢ Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).

➢ Damage from improper repair by unauthorized ART technicians.

➢ Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】; or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the PCI card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> PCI.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.